WHAT IS CLAIMED IS:

1. A method of manufacturing an insulated-gate semiconductor device having an SOI structure, said method comprising the steps of:

forming a crystalline semiconductor on an insulative substrate or an insulating layer;

forming a source region, a drain region and a channel forming region by using the crystalline semiconductor;

forming impurity regions artificially and locally in the channel forming region so that said channel forming region includes carrier moving regions and said impurity regions,

wherein said impurity regions are added with an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed; and

forming a gate insulating film and a gate electrode on the channel forming region.

2. A method of manufacturing an insulated-gate semiconductor device having an SOI structure, said method comprising the steps of:

forming a crystalline semiconductor on an insulative substrate or an insulating layer;

forming a source region, a drain region and a channel forming region by using the crystalline semiconductor;

forming impurity regions artificially and locally in the channel forming region so that the channel forming region includes carrier moving regions and the impurity regions wherein said impurity regions are added with an impurity element for shifting an energy band in such a direction that movement of holes is obstructed; and

forming a gate insulating film and a gate electrode on the channel forming region.

3. A method according to claim 1 or 2 wherein said impurity element is for forming a built-in potential difference locally in the channel forming region.

4. A method according to claim 1 wherein said impurity element belongs to group XIII.

5. A method according to claim 4 wherein said impurity element is boron.

6. A method according to claim 2 wherein said impurity element belongs to group XV.

7. A method according to claim 6 wherein said impurity element is phosphorus or arsenic.

8. A method according to claim 1 or 2 wherein said carrier moving regions are intrinsic or substantially intrinsic.

9. A method according to claim 8 wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than 5×10^{15} atoms/cm^3 and an oxygen concentration is less than 2×10^{18} atoms/cm^3.

10. A method according to claim 8 wherein the substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than 5×10^{15} atoms/cm^3 and an oxygen concentration is less than 1×10^{17} atoms/cm^3.

11. A method according to claim 1 or 2 wherein a width W of the channel forming region, a total width W_{pi} of the impurity regions, and a total width W_{pa} of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

12. A method according to claim 1 or 2 wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a

channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

13. A method according to claim 1 or 2 wherein the impurity regions serve as regions for buffering stress that occurs in the crystalline semiconductor.

14. A method according to claim 1 or 2 wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

15. A method according to claim 1 or 2 wherein said impurity regions have dot patterns.

16. A method according to claim 1 or 2 wherein said impurity regions have linear patterns substantially parallel with a channel direction.

17. A method according to claim 1 or 2 wherein said impurity element in said impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/cm^3.

18. An integrated circuit including a CMOS circuit having an n-channel field effect transistor and a p-channel field effect transistor, at least said n-channel field effect transistor having an SOI structure and comprising:

a crystalline semiconductor formed on an insulative substrate or an insulating layer, said crystalline semiconductor including a source region, a drain region and a channel forming region; and

a gate insulating film and a gate electrode formed on the channel forming region,

said channel forming region comprising:

carrier moving regions; and

impurity regions formed locally for pinning of a depletion layer developing from the drain region toward the channel forming region and the source region, said impurity regions containing an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed.

19. An integrated circuit including a memory circuit having a field effect transistor, said field effect transistor having an SOI structure and comprising:

a crystalline semiconductor including a source region, a drain region and a channel forming region; and

a gate insulating film and a gate electrode formed on the channel forming region,

said channel forming region comprising:

carrier moving regions; and

impurity regions formed locally for pinning of a depletion layer developing from the drain region toward the channel forming region and the source region, said impurity regions containing an impurity element for shifting an energy band in such a direction that movement of electrons is obstructed.

20. An integrated circuit according to claim 18 or 19, wherein said impurity element is for forming a built-in potential difference locally in the channel forming region.

21. An integrated circuit according to claim 19, wherein said impurity element belongs to group XIII.

22. An integrated circuit according to claim 21, wherein said impurity element is boron.

23. An integrated circuit according to claim 18 or 19, wherein said impurity element belongs to group XV.

24. An integrated circuit according to claim 23, wherein said impurity element is phosphorus or arsenic.

25. An integrated circuit according to claim 18 or 19, wherein said carrier moving regions are intrinsic or substantially intrinsic.

26. An integrated circuit according to claim 25, wherein said substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline

semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than 5 x 10^{15} atoms/cm^3 and an oxygen concentration is less than 2 x 10^{18} atoms/cm^3.

27. An integrated circuit according to claim 25, wherein said substantially intrinsic regions mean regions in which in the vicinity of a surface of the crystalline semiconductor a concentration of an impurity element for imparting one type of conductivity to the crystalline semiconductor is less than 5 x 10^{15} atoms/cm^3 and an oxygen concentration is less than 1 x 10^{17} atoms/cm^3.

28. An integrated circuit according to claim 18 or 19, wherein a width W of the channel forming region, a total width W_{pi} of the impurity regions, and a total width W_{pa} of regions between the impurity regions satisfy relationships $W_{pi}/W = 0.1$ to 0.9, $W_{pa}/W = 0.1$ to 0.9, and $W_{pi}/W_{pa} = 1/9$ to 9.

29. An integrated circuit according to claim 18 or 19, wherein in at least one cross-section taken by cutting the channel forming region in a direction perpendicular to a channel direction, the channel forming region is substantially regarded as a collection of a plurality of channel forming regions sectioned by the impurity regions.

30. An integrated circuit according to claim 18 or 19, wherein a reduction in threshold voltage caused by a short channel effect occurring in the channel forming region during driving is compensated by an increase in threshold voltage caused by a narrow channel effect obtained by utilizing the impurity regions.

31. An integrated circuit according to claim 18 or 19, wherein the impurity regions include means for buffering stress that occurs in the crystalline semiconductor.

32. An integrated circuit according to claim 18 or 19, wherein a total width of the carrier moving regions is within a range of 30 to 3,000 Å.

33. An integrated circuit according to claim 18 or 19, wherein said impurity regions have dot patterns.

34. An integrated circuit according to claim 18 or 19, wherein said impurity regions have linear patterns substantially parallel with a channel direction.

35. An integrated circuit according to claim 18 or 19, wherein a threshold voltage is controlled by controlling widths of the carrier moving regions.

36. An integrated circuit according to claim 18 or 19, wherein said impurity element in said impurity regions is at a concentration of $1x10^{17}$ to $1x10^{20}$ atoms/cm^3.

37. The integrated circuit of claim 18 or 19 in combination with at least an electric apparatus selected from the group consisting of a liquid crystal display device, an EL display device, a CL display device, a TV camera, a personal computer, a car navigation apparatus, a TV projection apparatus, a video camera, and a portable information terminal apparatus including a cellular telephone and a mobile computer.

38. A method according to claim 1, wherein said device is an EL display device.

39. An EL device having the integrated circuit according to claim 18.

40. An EL device having the integrated circuit according to claim 19.